

## High Efficiency 1.2MHz 28V 2A Step-up DC/DC Converter

### DESCRIPTION

The BL8042D is a constant frequency, current mode step-up converter intended for small, low power applications. The BL8042D switches at 1.2MHz and allows the use of tiny, low cost capacitors and inductors 2mm or less in height. Internal soft-start results in small inrush current and extends battery life.

The BL8042D includes under-voltage lockout, current limiting, thermal shutdown protection and output over voltage protection.

BL8042D is available in SOT23-6 package that is PB free.

### FEATURES

- 2.5V to 24V input voltage
- Up to 28V output voltage
- Accurate reference: 0.6V
- Integrated 150mΩ power MOSFET
- 1.2MHz switching frequency
- Internal 3A switch current limit
- Internal compensation
- Thermal shutdown
- Available in SOT23-6 package

### APPLICATIONS

- ABS set-top boxed
- DVB-S/S2

### TYPICAL APPLICATION

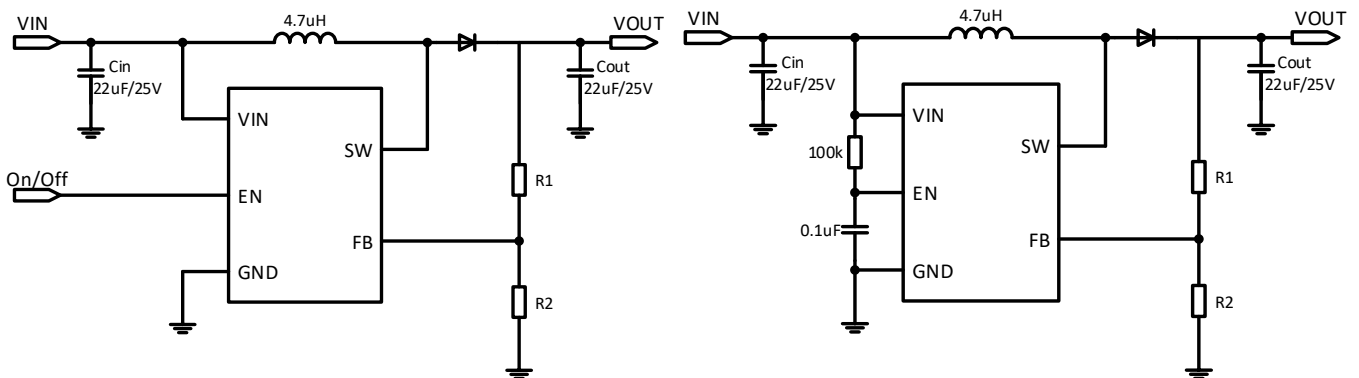


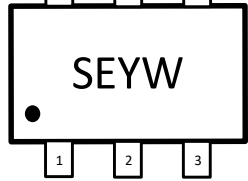
Figure1. BL8042D typical application circuit

### ORDERING INFORMATION

BL8042D [1](#) [2](#) [3](#)

Code	Description
1	Temperature & Rohs: C: -40~85°C, Pb free rohs std.
2	Package type: B6: SOT-23-6
3	Packing type: TR: tape & reel (standard)

### MARKING INFORMATION

Product classification		BL8042DCB6TR		
SEYW	Marking	NC	VIN	EN
	SE: product code	6	5	4
	YW: date code			
		SW	GND	FB

## PIN DESCRIPTION

Pin No.	Symbol	Description
1	SW	Power switch output. SW is the drain of the internal MOSFET switch. Connect the power inductor and output rectifier to SW. SW can swing between GND and 28V.
2	GND	Ground.
3	FB	Feedback input. The FB voltage is 0.6V. Connect a resistor divider to FB.
4	EN	Regulator On/Off control input. A high input at EN turns on the converter, and a low input turns it off. When not used, connect EN to the input supply for automatic startup.
5	VIN	Power supply. Must be locally bypassed.
6	NC	No connection

## ABSOLUTE MAXIMUM RATING

Parameter	Value	
VIN, EN pin voltage	-0.3V to 26V	
SW pin voltage	-0.3V to 26V	
All other pin voltage	-0.3V to 6V	
Junction temperature (T <sub>J</sub> )	150°C	
Power dissipation	600mW	
Thermal resistance (θ <sub>JA</sub> )	SOT23-6	250°C/W
Thermal resistance (θ <sub>JC</sub> )		130°C/W
Storage temperature (T <sub>S</sub> )	-65°C to 150°C	
Lead temperature & time	260°C, 10Sec	

## RECOMMENDED WORK CONDITIONS

Parameter	Value
Input voltage range	2.5V to 24V
Output voltage range	VIN to 28V
Operating ambient temperature (T <sub>A</sub> )	-40°C –85°C

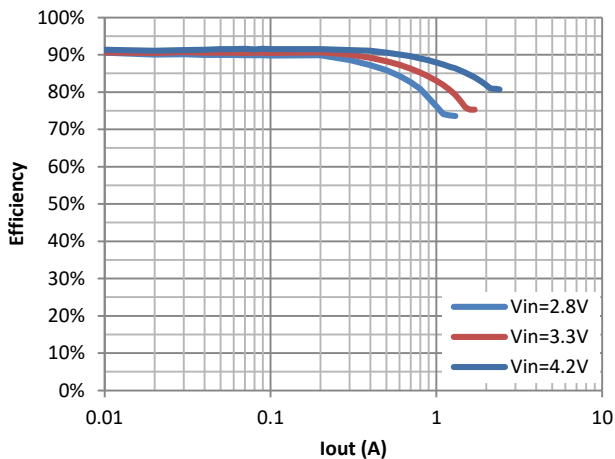
## ELECTRICAL CHARACTERISTICS

(Test Conditions: V<sub>IN</sub>=5V and V<sub>OUT</sub>=12V, L=4.7uH. Typical values are at T<sub>A</sub>=25°C, unless otherwise specified.)

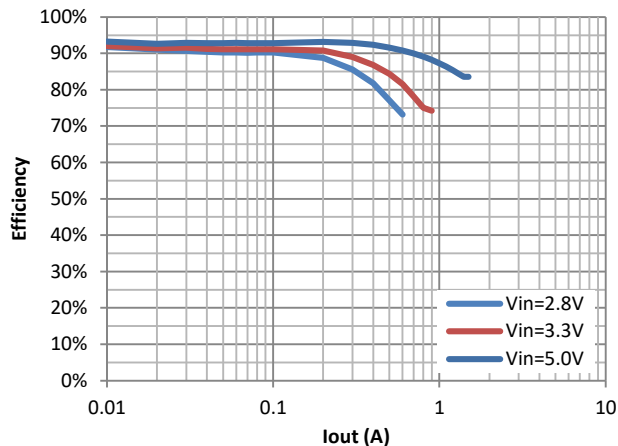
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>IN</sub>	Operating input voltage		2.5		24	V
V <sub>IN_UVLO</sub>	Under voltage lockout threshold	V <sub>IN</sub> rising		2.4		V
		V <sub>IN_UVLO</sub> hysteresis		50		mV
V <sub>FB</sub>	Feedback voltage		588	600	612	mV
I <sub>FB</sub>	FB input bias current	V <sub>FB</sub> =0.6V	-50	-10		nA
I <sub>SW_LKG</sub>	SW leakage	V <sub>SW</sub> =20V			1	uA
I <sub>Q</sub>	Quiescent current	V <sub>FB</sub> =0.8V, No switch		0.25	0.5	mA
		V <sub>EN</sub> =0V		0.1	1	uA
F <sub>SW</sub>	Oscillator frequency			1.2		MHz
T <sub>SS</sub>	Soft-start time			1.5		mS
D <sub>MAX</sub>	Maximum duty cycle			85		%
T <sub>ON(MIN)</sub>	Minimum ON time			120		ns
V <sub>EN_H</sub>	EN pin logic high threshold		1.0			V
V <sub>EN_L</sub>	EN pin logic low threshold				0.5	
R <sub>DS_ON</sub>	SW on-resistance			150		mΩ
I <sub>LIMIT</sub>	Current limit	V <sub>IN</sub> =5V, Duty cycle = 50%		3		A
T <sub>SD</sub>	Thermal shutdown			160		°C

## TYPICAL PERFORMANCE CHARACTERISTICS

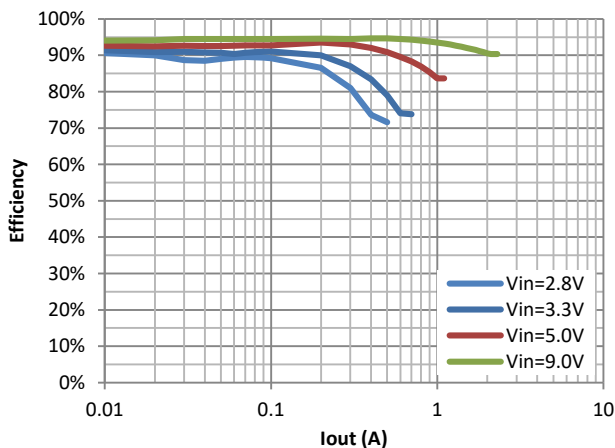
Efficiency vs. I<sub>out</sub>  
(V<sub>out</sub>=5V)



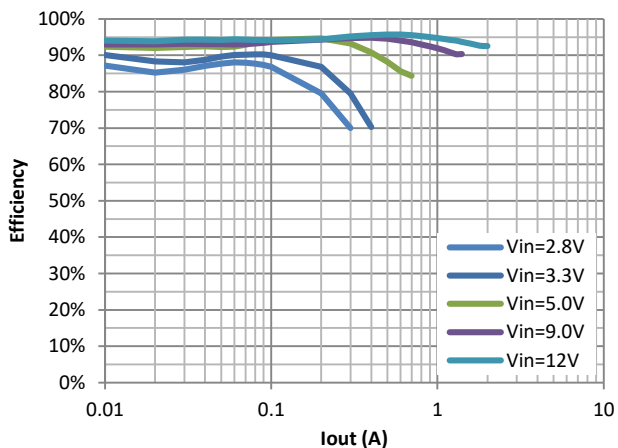
Efficiency vs. I<sub>out</sub>  
(V<sub>out</sub>=9V)



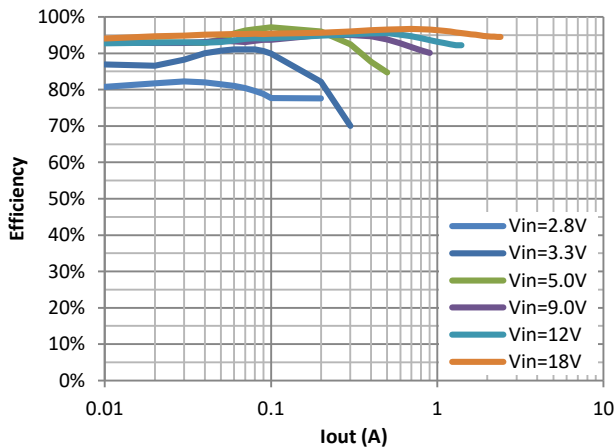
Efficiency vs. I<sub>out</sub>  
(V<sub>out</sub>=12V)



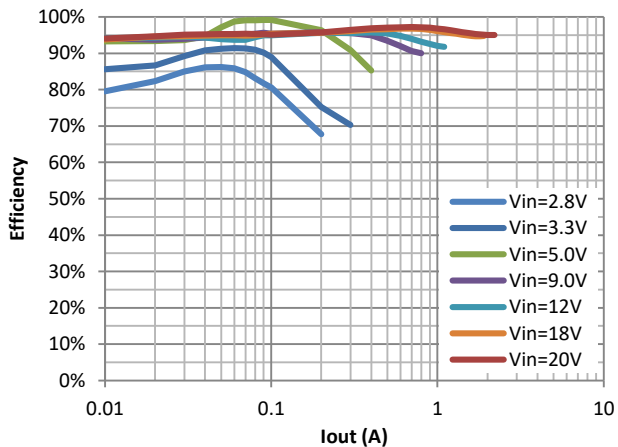
Efficiency vs. I<sub>out</sub>  
(V<sub>out</sub>=18V)



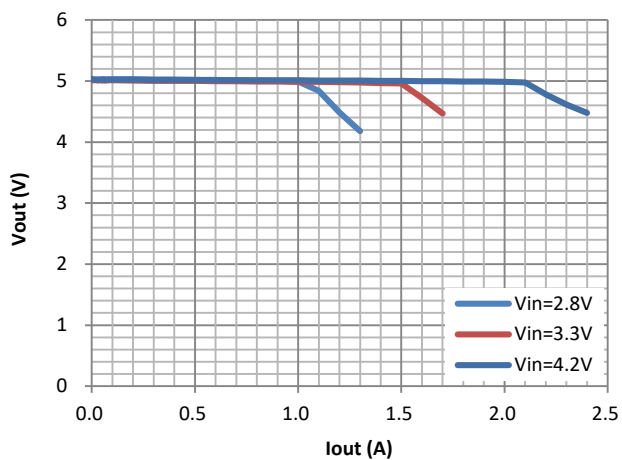
Efficiency vs. I<sub>out</sub>  
(V<sub>out</sub>=24V)



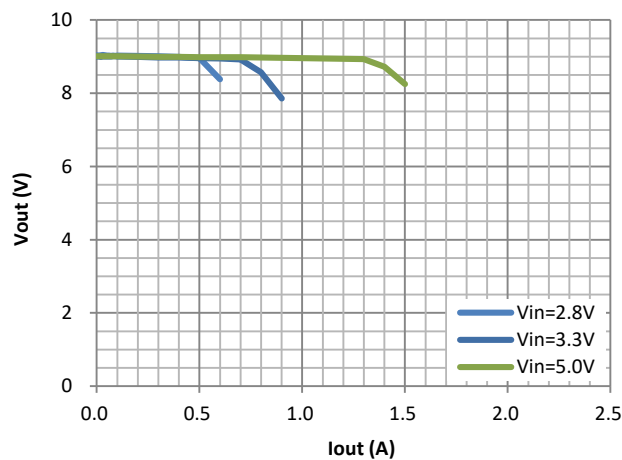
Efficiency vs. I<sub>out</sub>  
(V<sub>out</sub>=28V)



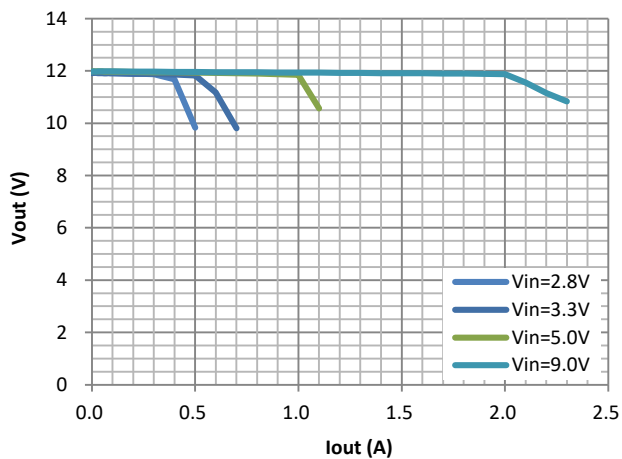
**Load Regulation  
(Vout=5V)**



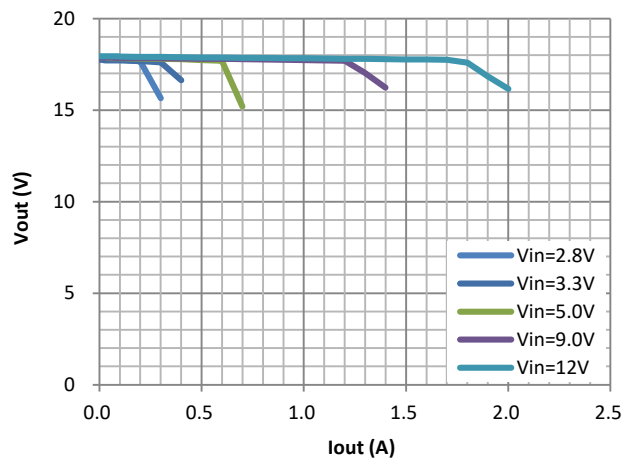
**Load Regulation  
(Vout=9V)**



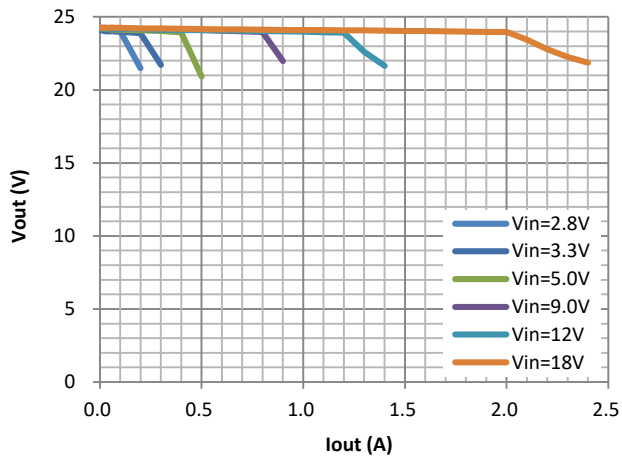
**Load Regulation  
(Vout=12V)**



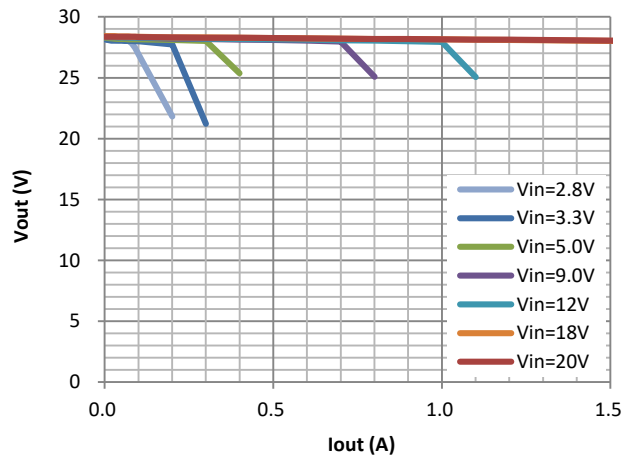
**Load Regulation  
(Vout=18V)**



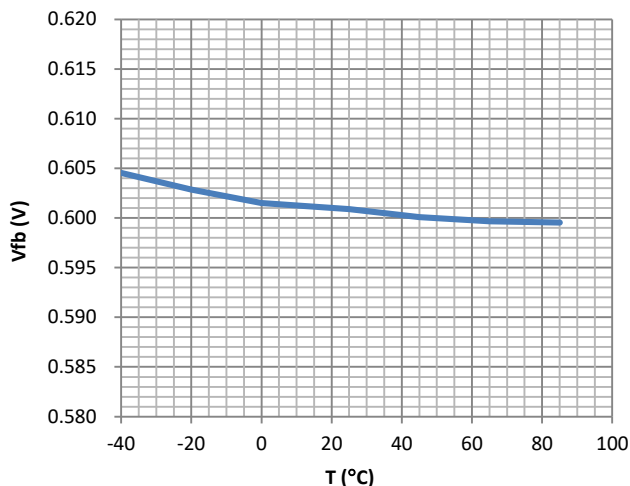
**Load Regulation  
(Vout=24V)**



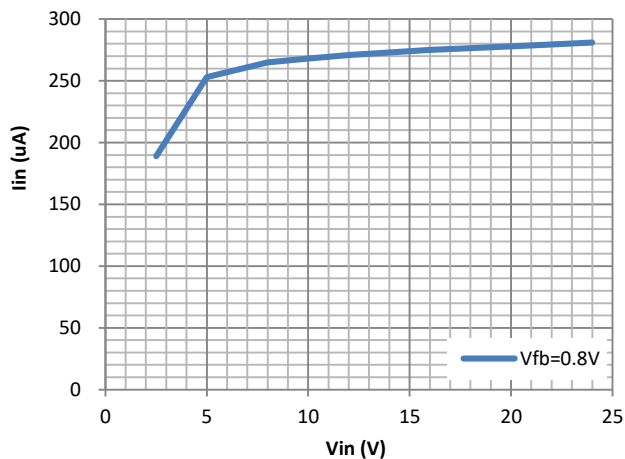
**Load Regulation  
(Vout=28V)**



### Vfb vs. Temperature

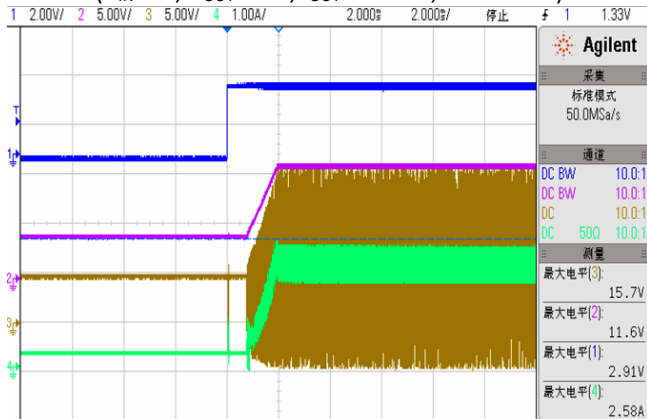


### Iq (No Switching)



### Enable Response

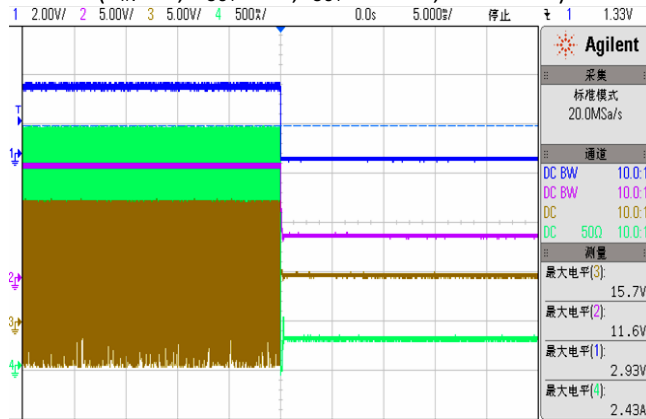
(VIN=5V, VOUT=12V, IOUT=800mA, EN=0→3V)



CH1: EN, CH2: Vout, CH2: Vsw, CH4: IL

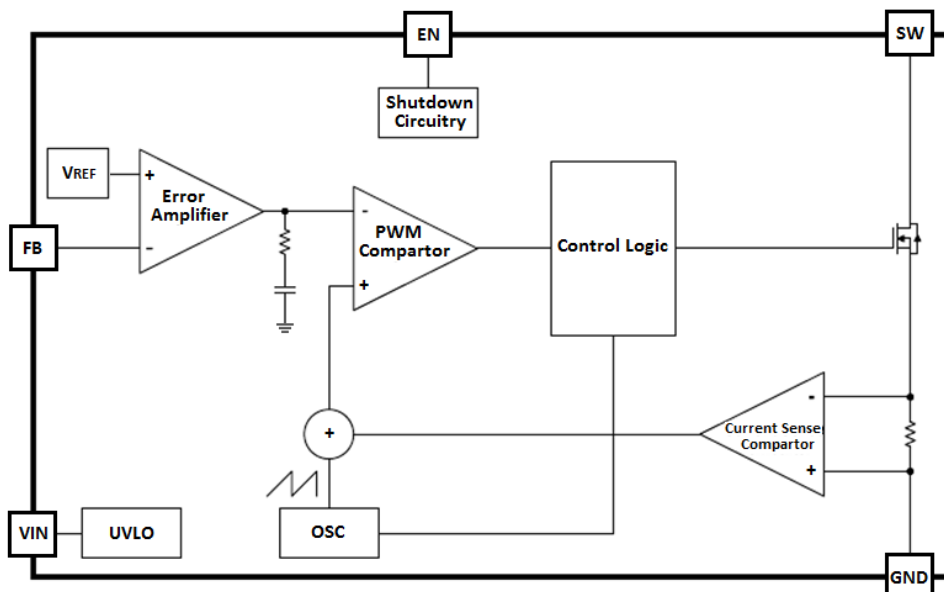
### Enable Response

(VIN=5V, VOUT=12V, IOUT=800mA, EN=3→0V)



CH1: EN, CH2: Vout, CH2: Vsw, CH4: IL

## BLOCK DIAGRAM



## DETAILED DESCRIPTION

The BL8042D uses a fixed frequency, peak current mode boost regulator architecture to regulate voltage at the feedback pin. The operation of the BL8042D can be understood by referring to the block diagram. At the start of each oscillator cycle the MOSFET is turned on through the control circuitry. To prevent sub-harmonic oscillations at duty cycles greater than 50 percent, a stabilizing ramp is added to the output of the current sense amplifier and the result is fed into the negative input of the PWM comparator. When this voltage equals the output voltage of the error amplifier the power MOSFET is turned off. The voltage at the output of the error amplifier is an amplified version of the difference between the 0.6V band

gap reference voltage and the feedback voltage. In this way the peak current level keeps the output in regulation. If the feedback voltage starts to drop, the output of the error amplifier increases. These results in more current to flow through the power MOSFET, thus increasing the power delivered to the output. The BL8042D has internal soft start to limit the amount of input current at startup and to also limit the amount of overshoot on the output. The BL8042D includes a number of protection features including under-voltage lockout, current limiting, thermal shutdown protection and output over voltage protection. Output voltage protection works when FB short to the GND.

## APPLICATION INFORMATION

### Setting the output voltage

The internal reference  $V_{REF}$  is 0.6V (Typical). The output voltage is divided by a resistor divider, R1 and R2 to the FB pin. The output voltage is given by

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$

### Inductor selection

The recommended values of inductor are 4.7 to 22 $\mu$ H. Small size and better efficiency are the major concerns for portable device, such as BL8042D used for mobile phone. The inductor should have low core loss at 1.2MHz and low DCR for better efficiency. To avoid inductor saturation current rating should be considered.

### Capacitor selection

Input and output ceramic capacitors of 22 $\mu$ F are recommended for BL8042D applications. For better voltage filtering, ceramic capacitors with low ESR are recommended. X5R and X7R types are suitable because of their wider voltage and temperature ranges.

### Diode selection

Schottky diode is a good choice for BL8042D because of its low forward voltage drop and fast reverse recovery. Using Schottky diode can get

better efficiency. The high speed rectification is also a good characteristic of Schottky diode for high switching frequency. Current rating of the diode must meet the root mean square of the peak current and output average current multiplication as following:

$$I_D(RMS) \approx \sqrt{I_{OUT} \times I_{PEAK}}$$

The diode's reverse breakdown voltage should be larger than the output voltage.

### Layout consideration

When laying out the printed circuit board, the following checking should be used to ensure proper operation of the BL8042D.

Check the following in your layout:

- 1) The power traces, consisting of the GND trace, the SW trace and the VIN, trace should be kept short, direct and wide.
- 2) Does the (+) plates of  $C_{in}$  connect to  $V_{in}$  as closely as possible. This capacitor provides the AC current to the internal power MOSFETs.
- 3) Keep the switching node SW away from the sensitive VOUT node.
- 4) Keep the (-) plates of  $C_{in}$  and  $C_{out}$  as close as possible

## PACKAGE OUTLINE

