PN8200

Chipown

X capacitor discharge IC

General Description

PN8200 is an automatic X capacitor discharge IC with two terminals, that could get low power consumption and meet safety standards. PN8200 built-in 1000V avalanche-rugged smart VDMOSFET, protecting the IC from damage. The chip checks AC voltage through the discharge resistors; when an AC mains voltage is applied, the very low current (15uA) flow in the discharge resistors to reduce power consumption to less than 5mW at 230VAC; when an AC mains voltage is disconnected, and a high voltage remains on the X capacitor, PN8200 automatically discharges the X capacitor by the discharge resistors. The discharge resistors and X capacitor could be chosen flexibly to optimize EMI performance.
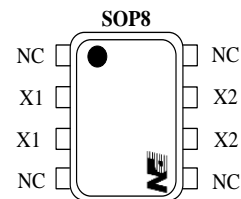
Features

- Internal 1000 V avalanche-rugged smart VDMOSFET
- No external ground pin leads to strong interference ability
- Blocks current through X capacitor when AC voltage is applied
- Automatically discharges the X capacitor when AC voltage is disconnected
- X capacitor could be chosen flexibly to optimize EMI design
- Self supplied and doesn't need external bias
- Two terminals and meets safety standards
- Discharge current internally limited
- Compliant to IEC 62368-1:2014
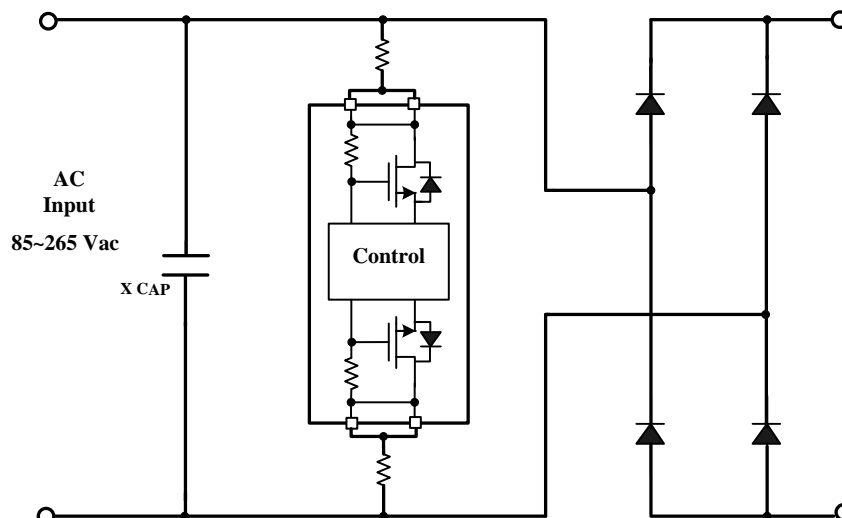
Applications

- All converters requiring very low no-load consumption or standby power
- Appliances requiring EuP Lot 6 compliance
- White Goods

Package/Order Information

SOP8

NC	NC
X1	X2
X1	X2
NC	NC

Order Code	Package
PN8200SEC-R1	**SOP8**

Typical Circuit

Pin Definitions

Pin Name	Pin Number	Pin Function Description
NC	1, 4, 5, 8	Unconnected Pin
X1	2, 3	AC Input1
X2	6, 7	AC Input2

Absolute Maximum Ratings

Pin X1,X2 ……………...……………… ……-0.3~1000V

Operating Junction Temperature ....…………..………-40~150℃

Storage Temperature Range …………...……………..……-55~150℃

Lead Temperature (Soldering, 10Secs)..…………....260℃

Package Thermal Resistance θ$_{JC}$ （SOP8）...……………….40℃/W

HBM ESD Protection [1]... ±2.5kV

Note：1.Test standard: ANSI/ESDA/JEDEC JS-001-2017.

Electrical Characteristics

(T_A = 25 ℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AC removal detection Time	T_{DET}	Line cycle frequency 47 to 63Hz		32		ms
Supply current	I_{OP}			15		uA
Discharge current limited	I_{CLP}		2.8		5	mA
VDMOS breakdown voltage	BV_{dss}	I_{X1-X2}=250uA	1000			V

Functional Description

PN8200 is an automatic X capacitor discharge IC with two terminals, and built-in 1000V avalanche-rugged smart VDMOSFET switch. The chip checks AC voltage through the discharge resistors, when an AC mains voltage is applied, the internal control will check the AC voltage zero crossings, and Block current through X capacitor discharge resistors; when an AC mains voltage is disconnected, PN8200 will automatically discharge the X capacitor by the series discharge resistors after Detection Time (TYP:32ms). The discharge current is determined by external discharge resistors, but the maximum discharge current is limited internally. The discharge resistors and X capacitor could be chosen flexibly, its time constant is set within 1 second normally.

Typical Application

Reference for matching the capacitance of X capacitor and resistance values of series resistors：
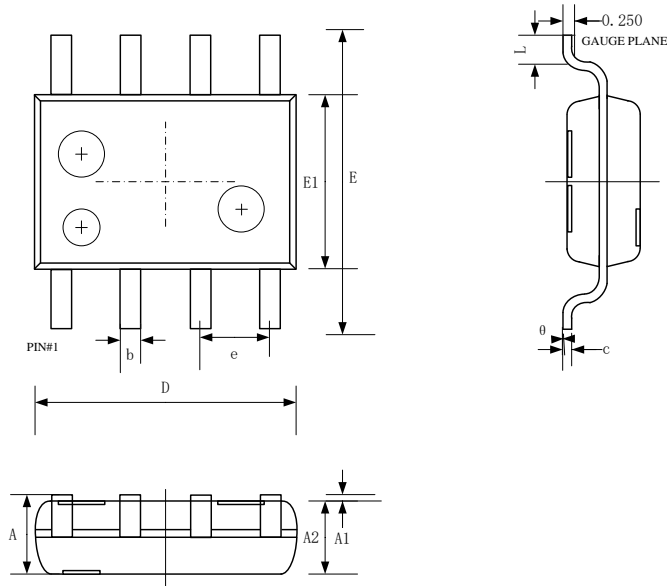
Capacitance of X capacitor	Resistance values of series resistors（RD1+RD2）	Capacitance of X capacitor	Resistance values of series resistors（RD1+RD2）
0.1uF	3.9MΩ+3.9MΩ	1uF	390kΩ+390kΩ
0.22uF	2.0MΩ+2.0MΩ	2.2uF	200kΩ+200kΩ
0.33uF	1.2MΩ+1.2MΩ	3.3uF	120kΩ+120kΩ
0.47uF	910kΩ+910kΩ	4.7uF	91kΩ+91kΩ
0.68uF	620kΩ+620kΩ	5.6uF	75kΩ+75kΩ
0.82uF	510kΩ+510kΩ	6.8uF	62kΩ+62kΩ

Component Parameter and Layout Considerations:

1. The MOV is placed in the input of power supply to reduce the voltage stress of X capacitor and the IC.
2. PN8200 is placed behind the MOV in the loop of PCB layout, so that the high voltage will pass through the MOV circuit first when the surge occurs, which can reduce the voltage stress of PN8200.
3. The total discharge resistor is suggested larger than 120kΩ, that could avoid the chip overheating in discharge condition.

PN8200

Package Information

SOP8 Package Information

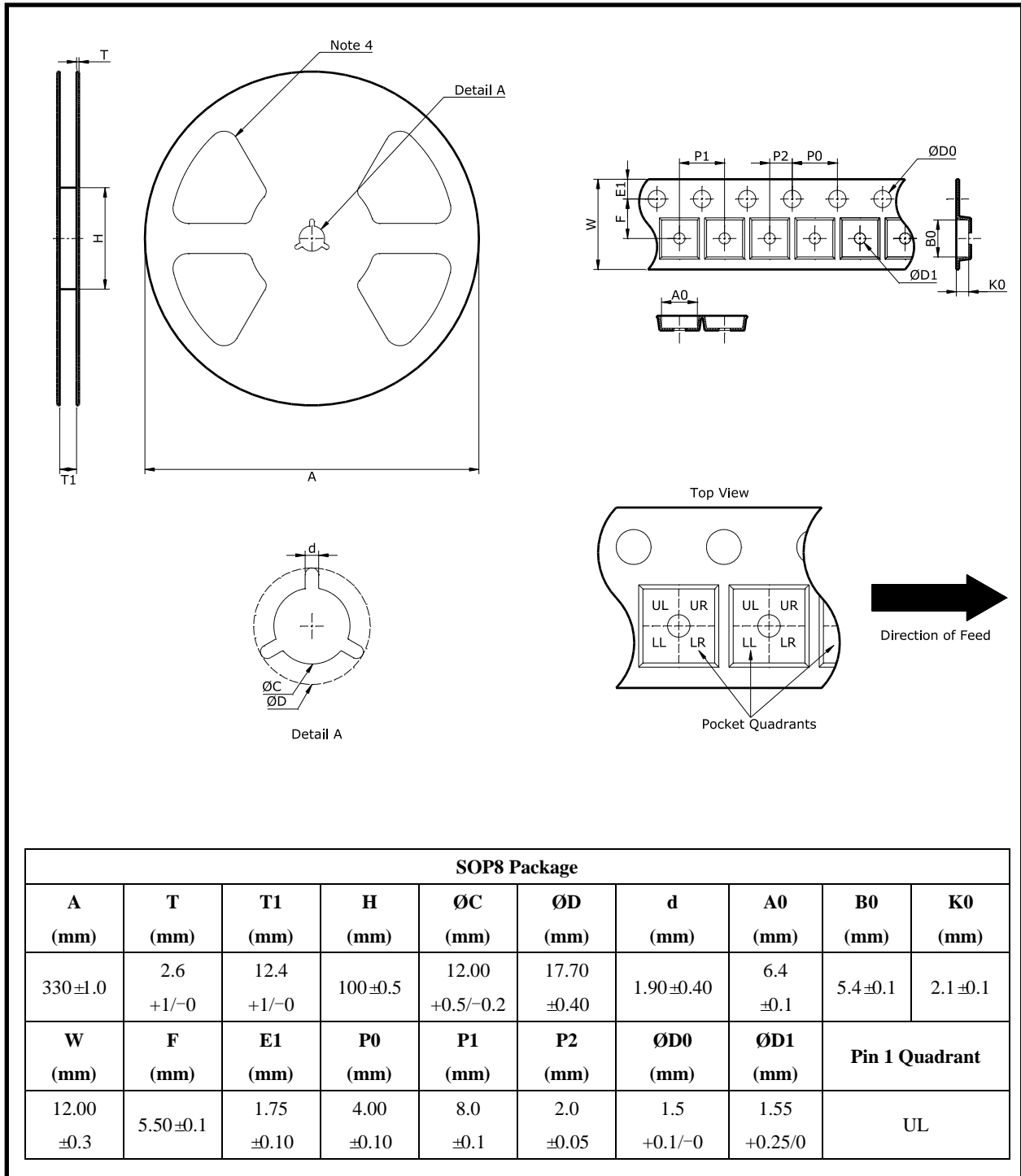| Size Symbol	Min. (mm)	Max. (mm)	Size Symbol	Min. (mm)	Max. (mm)
A	1.450	1.750	E	5.800	6.200
A1	0.100	0.250	E1	3.800	4.000
A2	1.350	1.550	e	1.270(BSC)	
b	0.330	0.510	L	0.400	1.270
c	0.170	0.250	θ	0°	8°
D	4.700	5.100			

Top mark	Package
PN PN8200 YWWXXXXX	SOP8
Note: Y: Year Code; WW: Week Code; XXXXX: Internal Code	

Notes:

1. This drawing can be adjusted without notice.

2. The device body size does not contain die flown.

Braid Tape And Reel Information

SOP8 Package									
A (mm)	**T** (mm)	**T1** (mm)	**H** (mm)	**ØC** (mm)	**ØD** (mm)	**d** (mm)	**A0** (mm)	**B0** (mm)	**K0** (mm)
330±1.0	2.6 +1/−0	12.4 +1/−0	100±0.5	12.00 +0.5/−0.2	17.70 ±0.40	1.90±0.40	6.4 ±0.1	5.4±0.1	2.1±0.1
W (mm)	**F** (mm)	**E1** (mm)	**P0** (mm)	**P1** (mm)	**P2** (mm)	**ØD0** (mm)	**ØD1** (mm)	**Pin 1 Quadrant**	
12.00 ±0.3	5.50±0.1	1.75 ±0.10	4.00 ±0.10	8.0 ±0.1	2.0 ±0.05	1.5 +0.1/−0	1.55 +0.25/0	UL	

Notes:

1. This drawing can be adjusted without notice.

2. All sizes are nominal values of mm.

3. This drawing is not strictly proportions, and is for reference only. Customers can contact Chipown sales for more details.

4. Examples here are for reference only.

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